

Performance Analysis of Static Carry Skip Adder Using 22nm Strained Silicon CMOS Technology.

D. Anisha Esther Annabai, E. Hemalatha, C. Divya, J. Ajayan, A. MuthuKumar and T. Ravichandran.*

Department of Electronics and Communication Engineering, SNS College of Technology, Coimbatore, India.

**Corresponding Author's Email: anishaesther96@gmail.com*

ARTICLE INFO

Article history:

Received : 09 Jan. 2018

Accepted : 24 Jan. 2018

Available online : 01 Feb. 2018

Keywords:

CMOS technology,
Carry Skip Adder,
High performance,
Low power supply.

ABSTRACT

A 256-bit adder was designed using 22nm Strained Silicon CMOS technology which is attractive for future VLSI and ULSI application. Carry Skip adders are widely used in cascaded circuit connection and it also improves the delay of the circuit compared to other adders. In this paper, the performance and an analysis on the delay, power, space and speed of strained CMOS technology based static carry skip adder will be presented. The circuits are simulated using 22-nm high performance CMOS with a low supply voltage of 0.8V using HSPICE software tool. The performance of the adder circuit is analyzed by measuring the key parameters of the circuit such as speed, power and also the effect of temperature on circuit performance is also analyzed.

© 2018 International Journal of Advanced Research in Science and Technology (IJARST).

All rights reserved.

PAPER-QR CODE



Volume 7, Issue 1

Citation: Anisha Esther Annabai. et. al. Performance Analysis of Static Carry Skip Adder Using 22nm Strained Silicon CMOS Technology. Int. J. Adv. Res. Sci. Technol. Volume 7, Issue 1, 2018, pp.732-735.

Introduction:

Adders are combinational circuits whose output entirely depends upon the input signals. High speed adders are configured according to desired complexity of arithmetic and numeric computation and are used in applications like ALU, digital signal processing and used in processor chips to find the address and table indices. In this, adders are designed using Static CMOS technology. Basically, in Static CMOS technology more number of transistors are used (2N number of transistors are required) to design a circuit. So that the circuit design occupies more area and it also reduce the speed of the circuit. Pull-up network (PUN) and Pull-down network (PDN) connected in series to form CMOS circuit design. N number of single bit full adders is connected in cascaded form to obtain Ripple carry adder (RCA). In Ripple carry adder, the carry out of first stage is given as input to the next succeeding stage. It needs to wait for the carry input signal and delay will occur. Ripple carry adder delay will overcome by Carry skip adder. Carry skip adders are preferred because compared with other adders it will reduce the delay of the circuit. Carry Skip adder is the fastest circuit design. By reducing width of the transistors level, the speed is increased. Increase in delay leads to the reduction in power obtained. In Carry

skip adder the delay depends on the gate delay and number of bits used. Area occupied and power supplies used are the most important factors in a circuit design. Further concepts are describes as follows. Section II shows the structure of Static carry skip adder. Simulation results are obtained in section III. Summarized work shown in Section IV.

Structure of Static Carry skip adder:

Carry skip adders are preferred because compared with other adders it will reduce the delay of the circuit. The Carry skip is designed using Static CMOS technology so that it occupies more area. The Static CMOS design is as follows: If the equation is in AND form means PMOS should connect in parallel else the equation is in OR form means PMOS should connect in series. Likewise if the equation is in AND form means NMOS should connect in series else the equation is in OR form means NMOS should connect in parallel. In this, a 256-bit adder is designed using 22-nm strained silicon CMOS technology and it uses the supply voltage 0.8V.

A. Conventional Carry Skip Adder:

The Schematic diagram of Conventional Carry skip adder is shown in Fig. 1. The Conventional Carry skip adder consists of four block of full adders (RCA block),

four two input EX-OR gates, Single four input AND gate and Single 2:1 Multiplexer. Here four-bit Conventional Carry skip adder is designed using Static CMOS technology. To design a Single bit full adder 46 transistors are needed. Four block of Single bit full adder combine to form a Ripple carry adder. The function of Ripple carry adder is given as N number of full adders connected cascaded form ripple carry adder. Totally 184 transistors are needed to design a ripple carry adder. Totally 246 transistors are needed to design Conventional Carry skip adder. The function of EX_OR gate is if both the input is high or if both the input is low, the output is zero. Otherwise the output will be high. Likewise it performs the operation and produces the output Y0, Y1, Y2, Y3.

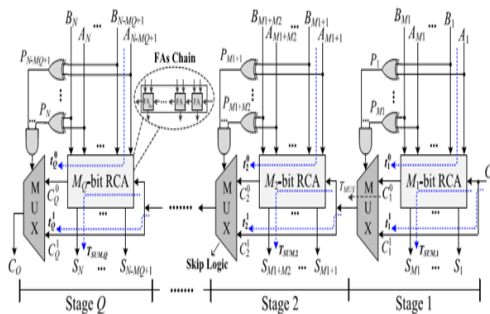


Fig. 1: Schematic diagram of Conventional Carry skip adder

These outputs are given a input to the AND gate and produces the output P0 ($P_0 = Y_0, Y_1, Y_2, Y_3$). Then P0 will be the select line of 2:1 MUX. The Ripple carry adder block output Carry C3 and input (C_{in}) are the inputs of 2:1 MUX and it produces the output (C_{out}). The value of C_{out} can be calculated as

$$C_{out} = P_0 \cdot C_{in} + \overline{P_0} \cdot C_3$$

If the P0 value is one directly C in is given as input to 2:1 MUX. If the P0 value is zero then it perform the operation of Ripple carry adder block and its carry C3 is given as input to 2:1 MUX from that output is calculated.

B. Proposed Carry Skip Adder:

The Schematic diagram of Proposed Carry skip adder is shown in Fig. 2. The proposed Carry skip adder consists of input bits from A0-A7, B0-B7 and C_{in} . The proposed 8-bit Carry skip adder is designed using 22-nm Strained Silicon CMOS technology. For a Single bit full adder 46 transistors are needed. For 8-bit adder 368 are needed. Totally 460 transistors are needed to design Proposed 8-bit Carry skip adder. So that it requires more number of transistors and it occupies more space. Delay will occur while performing the function. Compare with Conventional Carry skip adder proposed Carry Skip adder is best. The function of Proposed Carry skip adder is each stage consists of two input bits A, B and RCA block. The first stage performs the

operation and produces the output sum and carry where the carry of first block is given as C_{in} to the next stage. Simultaneously compute for all stages, in this first stage consists of one block (RCA) and other block consists of RCA block and incrementation block.

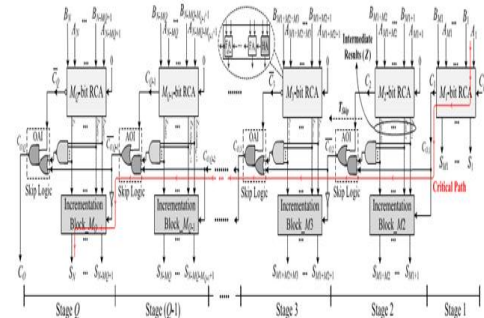


Fig. 2: Schematic diagram of Proposed Carry Skip adder

Simulation Results:

The Simulation results using HSPICE software tool in high performance and low power 22-nm Strained Silicon CMOS technology at a temperature from 27⁰C to 107⁰C for four-bit Conventional Static and eight-bit Proposed CSKA. The supply voltage used in the simulation is 0.8V. Fig.3 shows the input waveform of four-bit Conventional Static CSKA. Fig.4 shows the output waveform of four-bit Conventional Static CSKA. Fig.5 shows the input waveform of eight-bit Proposed Static CSKA. Fig.6 shows the output waveform of eight-bit Proposed Static CSKA. Fig.7 shows the effect of temperature of four-bit Conventional Static CSKA. Fig.8. shows the effect of temperature of eight-bit Proposed Static CSKA. The effect of temperature of Static Carry skip adder sweeps from 27⁰C to 107⁰C). From Fig. 7 it is found that when the temperature is 27⁰C, the delay is 82ps and the power obtained is 54 microwatt. When the temperature is 107⁰C, the delay is 101.4ps and the power obtained is 45.3 microwatt. From Fig. 8 It is found that when the temperature is 27⁰C, the delay is 104.6ps and the power obtained is 104 microwatt. When the temperature is 107⁰C, the delay is 135.8ps and the power obtained is 85.9 microwatt. It has shown that as the temperature increases due to the reduction in actual power.

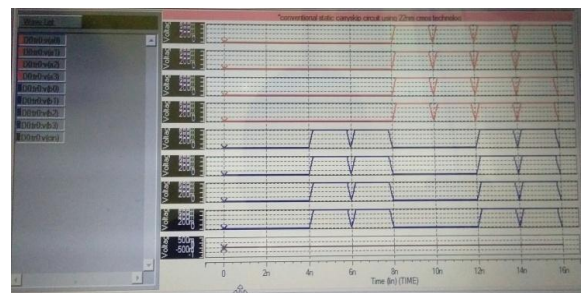


Fig. 3: Input Waveform of 4-bit Conventional Static Carry Skip Adder

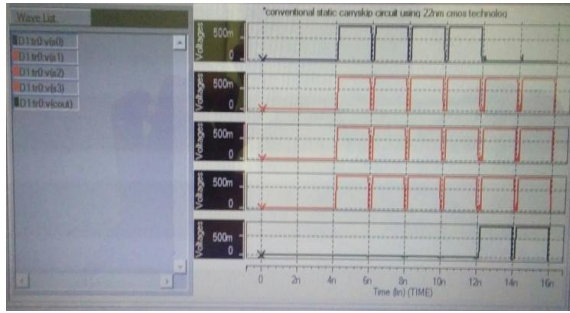


Fig. 4. Output Waveform of 4-bit Conventional Static Carry Skip Adder

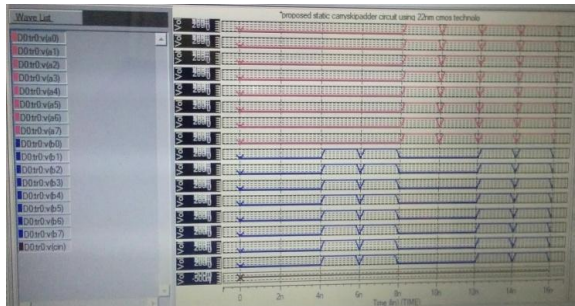


Fig. 5. Input Waveform of 8-bit Proposed Static Carry Skip Adder

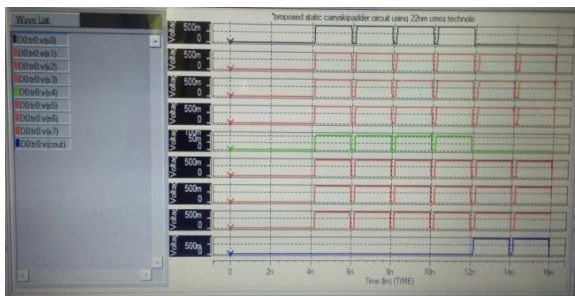


Fig. 6. Output Waveform of 8-bit Proposed Static Carry Skip Adder

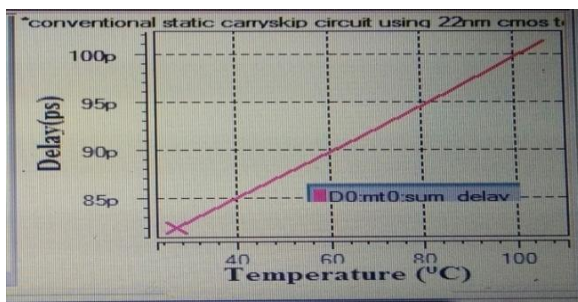


Fig. 7. Delay Vs Temperature Characteristics of Conventional Static Carry Skip Adder Using 22nm CMOS technology

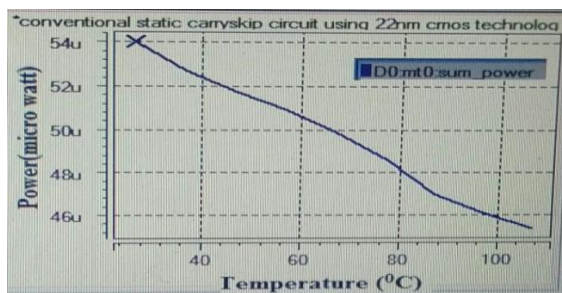


Fig. 8. Delay Vs Temperature Characteristics of Conventional Static Carry Skip Adder Using 22nm CMOS technology

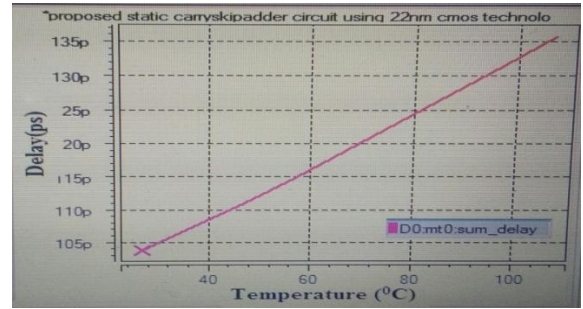


Fig. 9. Delay Vs Temperature Characteristics of Proposed Static Carry Skip Adder Using 22nm CMOS technology

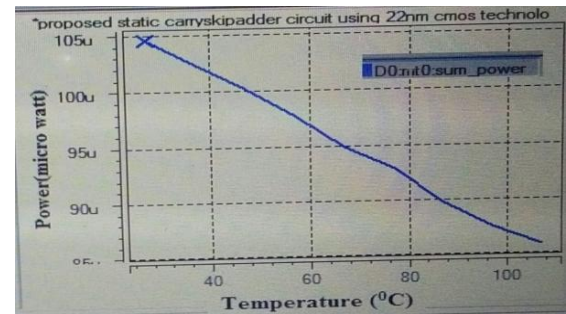


Fig. 11. Power Vs Temperature Characteristics of Proposed Static Carry Skip Adder Using 22nm CMOS technology

Table I compares the performance of the above mentioned Static Carry Skip adder

Table: 1. Performance of the static carry skip adder using 22nm strained Silicon CMOS Technology.

Adder Type	Static Conventional Adder		Static Proposed Adder	
	Delay (ps)	Power (microwatt)	Delay (ps)	Power (microwatt)
4Bit Adder	101.4	45.3	-	-
8Bit Adder	202.8	90.6	135.8	85.9
16Bit Adder	405.6	181.2	271.6	171.8
32Bit Adder	811.2	362.4	543.2	343.6
64Bit Adder	1622.4	724.8	1086.4	687.2
128Bit Adder	3244.8	1449.6	2172.8	1374.4
256Bit Adder	6489.6	2899.2	4345.6	2748.8

Conclusion:

In this paper, we presented the performance comparison of Carry skip adders designed using Static CMOS technology by using 22-nm Strained Silicon CMOS technology. The effect of temperature on the Static Carry skip adder is also analyzed by sweeping the temperature from 27(°C) to 107(°C). The Performance and analysis of 256-bit Conventional and Proposed Carry skip adder is mentioned in the table. The Simulation results are obtained using HSPICE software tool. Analysis shows that as the temperature increases, the delay of the circuit also increases due to the reduction in actual power.

References:

1. C. Nagendra, M.J. Irwin and R. M. Owens, "Area-time-power tradeoffs in parallel adders,"IEEE Transaction. Circuits System. II, Analog Digit. Signal Process, Volume.43, number. 10, pp.689-702Oct.1996.

2. C.H. Chang, J. Gu and M.Zhang, "A review of 0.18 μm full adder performances for tree structured arithmetic circuits," IEEE Transaction. Very Large Scale Inegr.(VLSI)SystemVolume.13,number.6,pp.686-695,Jun.2005.
3. D. Harris, "A taxonomy of parallel prefix networks," in Proc. IEEE Conference Rec 37th Asilomar Conference Signals System Comput., volume 2 Nov. 2003, pp 2213-2217.
4. High-Speed and Energy-Efficient Carry Skip Adder Operating Under a Wide Range of supply voltage levels Milad Bahadori, Mehdi Kamal, Ali Afzali-Kusha, Senior Member, IEEE and Massoud Pedra Fellow, IEEE.
5. K. Chirca et al., "A Static low-power, high-performance 32-bit carry skip adder," in Proc, Euromicro Symp. Digit. Syst. Design (DSD), Aug/Sep 2004, pp. 615-619.
6. M. Alioto and G. Palumbo, "A Simple strategy for optimized design of one-level carry-skip adders," IEEE Transaction Circuits System I, Fundamental theory. Application, volume. 50, number. 1, pp 141-148, Jan 2003.
7. M. Lehman and N. Burla, "Skip techniques for high-speed carry propagation in binary arithmetic units," IRE Transaction. Electron. Comput.,Volume. EC-10, number 4, pp.691-698, Dec 1961.
8. M. Vratonjic, B.R Zeydel and V.G. Oklobdzija, "Low and ultralow-power arithmetic units: Design and comparison," in Proc. IEEE International Conference. Comput. Design, VLSI Comput Process,(ICCD),Oct.2005,pp.249-252.
9. P.K. Chan, M.D.F Schlag, C.D. Thomborson and V.G. Oklobdzija, "Delay optimization of carry-skip adders and block carry-look ahead adders using multidimensional dynamic programming," IEEE Transaction Comput., volume. 41, number. 8, pp 920-930, Aug.1992.
10. P.M. Kogge and H.S. Stone," A parallel algorithm for the efficient solution of a general class of recurrence equations," IEEE Transaction Comput., volume C-22 number 8 pp.786-793, Aug 1973.
11. R.P. Brent and H.T. Kung, "A regular layout for parallel adders," IEEE Transaction. Comput., volume C-31 number 3 pp. 260-264, March 1982.
12. S. Turrini, "Optimal group distribution in carry-skip adders," in proc. 9th IEEE Symp. Comput. Arithmetic, Sep. 1989,pp. 96-103.