Int. J. Adv. Res. Sci. Technol. Volume 4, Issue 5, 2015, pp.481-484.

IJARST

International Journal of Advanced Research in Science and Technology

journal homepage: www.ijarst.com

ISSN 2319 – 1783 (Print)

ISSN 2320 – 1126 (Online)

Implementation of a 4T DRAM element for faster digital system applications.

Vamsi. J and B. Rambabu*

Department of ECE, Koushik Engg College,Visakhapatnam, Andhra Pradesh, India.

****Corresponding Author's Email:*** *vamsikrishna.jonnada@gmail.com*

A R T I C L E I N F O

Article history:

Received 01 Jun. 2015

Accepted 24 Jun. 2015

Available online 10 Aug. 2015

Keywords:

One Transistor (1T),
4 Transistor (4T),
Dynamic RAM (DRAM)

PAPER-QR CODE

IJARST
Volume-4, Issue-5

A B S T R A C T

This paper deals with analysis of average power consumption of dram cell designs for the nanometer scale memories. These DRAMs are used in many modern processors' internal memory. The major contributor of power in dram is the off state leakage current. Improving the power efficiency of a dram cell is critical for the improvement in average power consumption of the overall system. 3T dram cell, 4T dram cells are designed by using TANNER EDA tool and their average power consumption are compared. Average power consumption, write access time, read access time and retention time of 4T, 3T DRAM cell are simulated and compared on 32 nm technology.

Citation: *Vamsi. et al. Implementation of a 4T DRAM element for faster digital system applications. Int. J. Adv. Res. Sci. Technol. Volume 4, Issue 5, 2015, pp.481-484.*

Introduction:

Performance of modern computer systems has seen dramatic improvements in the past thirty years due to advancements in silicon process technology. The advancements in silicon process technology have enabled the number of transistors on a single chip to roughly double every two years as suggested by Moore's Law. As a corollary to Moore's Law, processor performance has also doubled roughly every two years in the same time period due to a combination of the larger transistor budget and the increased switching speed of those transistors. However, increases in processor performance did not lead to comparable increases in performance of computer systems for all types of applications. The reason that increases in processor performance did not lead directly to comparable increases in computer system performance is that computer system performance is fundamentally constrained by the interaction between the processor and memory elements. Moreover, in contrast to the rapid improvements in processor performance, memory system performance has seen only relatively modest improvements in the past thirty years. The result of the imbalance in performance scaling trends between processor and memory is that modern computer systems are increasingly constrained by the performance of memory systems; in particular, the performance of DRAM based memory systems. The work in this dissertation is dedicated to the investigation of DRAM memory system performance characteristics, and the result of the investigation is then used to evaluate and support the design of future DRAM devices.

With microprocessors getting faster every year, memory architectures must also improve to enhance the overall system performance.

The work in this dissertation is dedicated to the investigation of DRAM memory cell design with higher efficiency and integrity. System performance characteristics and the result of the investigation is then used to evaluate and support the design of future DRAM design. Overall book is divided into three sections. The first section briefly reviews the DRAM basics. Next section deals with DRAM device architecture. The final section shows implementation of efficient DRAM and the simulation results.

DRAM Device Architecture and design:

To facilitate the study of DRAM based memory systems, this section describes basic circuits and architecture of DRAM devices. The goal in this section is to provide a broad overview of functionalities of circuits and common functional blocks in DRAM devices sufficient to provide a basic understanding of

internal circuits and architecture of modern DRAM devices. With the understanding of the fundamentals of DRAM device operations in place, more advanced discussions of architectural trade-offs at the DRAM device and system level would then be possible. Various components such as DRAM storage cells, DRAM array structure, voltage sense amplifiers, control logic and decoders are then examined separately.

DRAM Device Organization:

Figure 2.1 illustrates the organization and structure of a Fast Page Mode (FPM) DRAM device. Internally, the array of DRAM storage cells in Figure 2.1 is organized as 4096 rows, 1024 columns per row, and 16 bits of data per column. In this device, each time a row access occurs, a 12 bit address is placed on the address bus and the row address strobe (RAS) is asserted by an external memory controller. Inside the DRAM device, the address on the address bus is buffered by the row address buffer, then sent to the row decoder. The row address decoder then accepts the 12 bit address and selects one of 4096 rows of storage cells. The data values contained in the selected row of storage cells are then sensed and maintained in the array of sense amplifiers. Each row of DRAM cells in this chip consists of 1024 columns and each column is 16 bits wide. That is, a 16 bit wide column is the basic addressable unit of memory in this device, and each column access that follows the row access would ordinarily read or write 16 bits of data from the same row of DRAM. The FPM DRAM device does allow each 8 bit half of the 16 bit column to be accessed independently through the use of separate column access strobe high (CASH) and column access strobe low (CASL) signals.

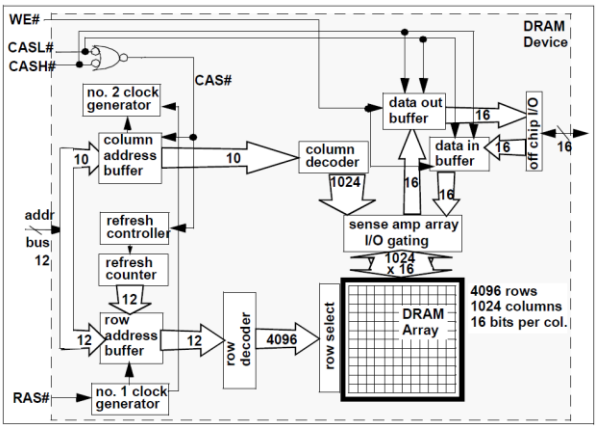


Fig. 1: 64 Mbit Fast Page Mode DRAM Device

(4096 x 1024 x 16).

The way that a column access is engaged is similar to the row access in that the memory controller would place a 10 bit address on the address bus, but then assert the appropriate column access strobe (CAS#) signals. Internally, the DRAM chip then takes the 10 bit column address, decodes it and uses it to select one column out of 1024 columns. The data for that column is then placed onto the data bus or overwritten with data from the data bus depending on the **write enable** (WE) signal. Finally, advanced DRAM devices such as ESDRAM, Direct RDRAM and RLDRAM have evolved to include more logic circuitry and functionality on chip, such as row caches or write buffers that allow for read-around-write functionality. These circuitry improve performance but add to the die cost of the DRAM device. As a result, they are not found in standard DRAM devices. However, these performance enhancing features may prove to be necessary elements in future high data rate DRAM devices.

DRAM Storage Cells:

Figure 2.2 shows a circuit diagram of the basic one transistor, one capacitor (1T1C)cell structure used in modern DRAM devices as the basic storage unit. In the structure illustrated in Figure 2.2, when the access transistor is turned on by applying a voltage on the gate of the access transistor, a voltage representing the data value may be placed onto the bitline and used to charge the storage capacitor.

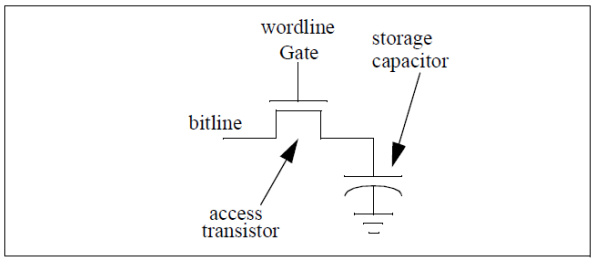


Fig. 2: Basic 1T1C DRAM Cell Structure.

The storage capacitor then retains the stored charge for a limited period of time after the voltage on the word line is removed and the access transistor is turned off. However, due to leakage currents through the access transistor, the electrical charge stored in the storage capacitor gradually dissipates. As a result, before the stored charge decays to indistinguishable values, data stored in DRAM cells must be periodically read-out and written back in a process known as ***refresh***. Otherwise, the stored electrical charge will gradually leak away and the value stored in the capacitor will no longer be resolvable after some time. In DRAM devices, large numbers of DRAM cells are grouped together to form DRAM array structures.

Differential Sense Amplifier:

In DRAM devices, the functionality of resolving small electrical charges stored in storage capacitors into digital values is performed by a differential sense amplifier. In essence, the differential sense amplifier takes the voltages from a pair of bitlines as input, senses the difference in voltage levels between the bitline pairs and amplifies the difference to one extreme or the other.

Functionality of Sense Amplifiers in DRAM Devices:

Sense amplifiers in modern DRAM devices perform three different functions. The first function that sense amplifiers perform in a DRAM device is to sense the

minute change in voltage that occurs when an access transistor is turned on and a storage capacitor places its charge on the bitline. The second function of sense amplifiers in a modern DRAM device is that sense amplifiers also restores the value of a cell after the voltage on the bitline is sensed and amplified. The third and somewhat surprising function of sense amplifiers in a modern DRAM device is that arrays of sense amplifiers also act as temporary data storage.

Circuit Diagram of a Basic Sense Amplifier:

Figure 2.4 shows the circuit diagram of a basic sense amplifier. Complex sense amplifiers in modern DRAM devices contain the basic elements shown in Figure 2.4 as well as additional circuit elements for array isolation, careful balance of the sense amplifier structure, and faster sensing capability.

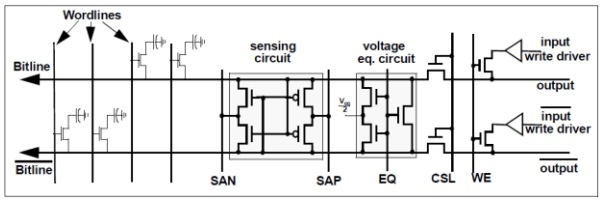


Fig. 3: Basic sense amplifier circuit diagram.

In the basic sense amplifier circuit diagram shown in Figure 2.4, the **equalization (EQ)** signal line controls the voltage equalization circuit. functionality of this circuit is to ensure that the voltages on the bitline pairs are as closely matched to each other as possible. Since the differential sense amplifier is designed to amplify the voltage differential between the bitline pairs, any voltage imbalance that exists on the bitline pairs prior to the activation of the access transistors would degrade the effectiveness of the sense amplifier.

Voltage Waveform of Basic Sense Amplifier Operation:

Figure 2.4 shows the voltage waveforms for the bitline and selected control signals illustrated in Figure 2.5. The bitline is pre charged, and the voltage on the bitline is set to the reference voltage, Vref. In phase one, the wordline voltage is overdriven to at least Vt above Vcc, and the DRAM cell discharges the content of the cell onto the bitline and raises the voltage from Vref to Vref+.

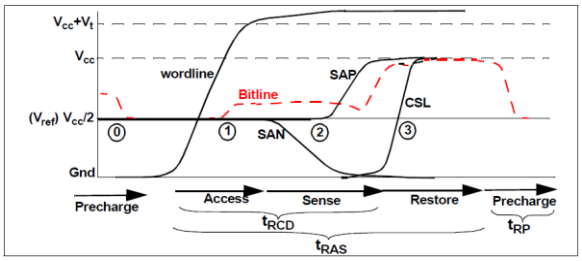
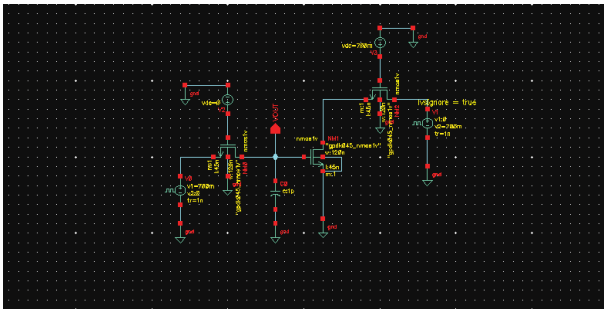


Fig. 4: Sense Amplifier READ cycle

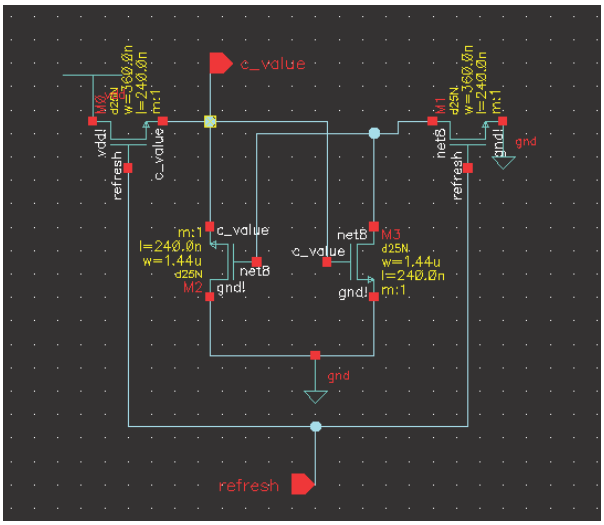
In phase two, the sense control signals SAN and SAP are activated in quick succession and drive the voltage on the bitline to the full voltage. The voltage on the bitline then restores the charge in the DRAM cells in phase three. After time tRCD, the sensing operation is complete, and the data can be read out through the DRAM device's data I/O after that time. However, after time period of tRCD from the beginning of the activation process, data has yet to be restored to the DRAM cells. After time period of tRAS from the beginning of the activation process, the data restore operation is assumed to be complete, and the DRAM device is ready to accept a precharge command that will complete the entire row cycle process after time period of t_{RP}.

A similar way follows for write operation

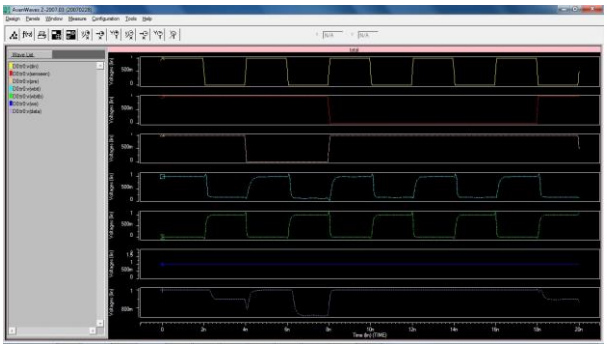
Simulation Results:



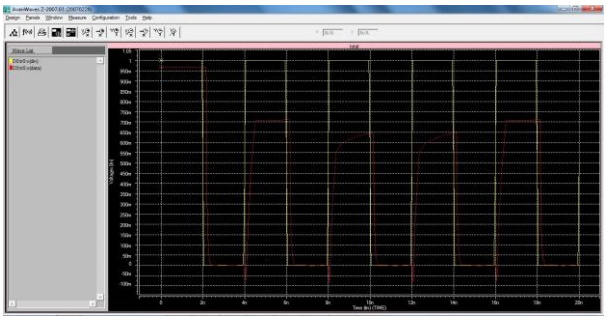
Schematic of 3T DRAM cell



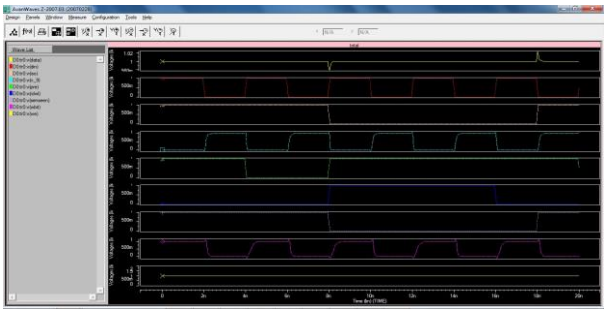
Schematic of 4T DRAM cell



1T DRAM Read Logic

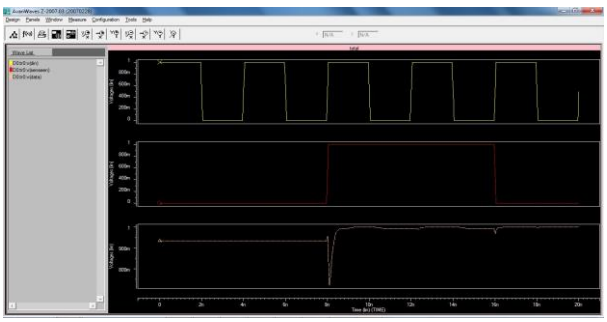


1T DRAM Write Logic

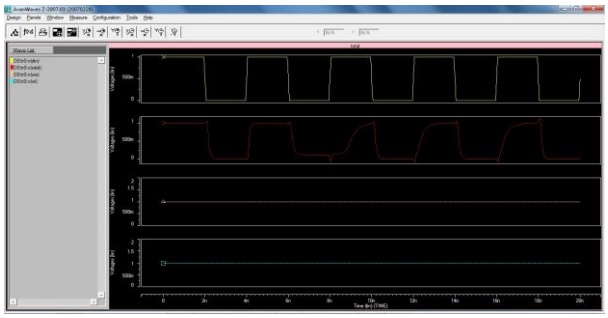


3T Read

3T Write



4T Read



4T Write

Write Operation

DRAM	Power dissipation	Delay
1T	29mw	6.9ns
2T	31.2mw	6.9ns
3T	44.8mw	5.8ns
4T	58.6mw	10.6ns

Read Operation

DRAM	Power dissipation	Delay
1T	41.6mw	9.2ns
2T	61.1mw	10.1ns
3T	52.6mw	6.1ns
4T	71.6mw	13.2ns

Conclusion:

For the implemented design the simulations were performed. Read, Write circuit timing diagrams of 4T DRAM cell have shown considerable improvement. Power and delay measurements show almost nearer values. Hence we could achieve higher architecture with good operation characteristics.

References:

1. Syam Akashe et.al, "Analysis of power in 3T DRAM nd 4T DRAM in different technology", World Congress on Information and Communication Technologies 2012.
2. Pooran Singh et.al, "Design of high speed DDR SDRAM controller with less logic utilization" International Conference on Devices, Circuits and Systems (ICDCS),2014
3. Prateek Asthana et.al,"Performance comparision of 3T and 4T DRAM cell design on 32nm technology", CS & IT-CSCP 2014