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Design of an efficient and faster SDRAM Controller.

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A B S T R A C T

In this paper Double data rate synchronous dynamic (DDR SDRAM) accessing of memory and controller are designed in such a way that it supports double data transfer rate. To guarantee that the system works as intended, the memory controller is configured such that all the real-time requirements of all sharing applications are satisfied. A fully functional DDRSDRAM controller is designed to perform Read and Write operations on both rising and falling edge (DDR) of clock from the memory by using data path module with double data transfer throughput and bandwidth of the memory. The implementation uses direct clocking for data capture. To improve the access speed controller will generate the control signals at high speed and memory also supposes to access the data very easily. The memory has been designed to access the data by using the CAS and RAS signals in an easy way and controller also has been implemented with double data rate. For a single row different column data can be read at a time so the improvement of 28.57% in the performance of memory accessing.

Introduction:

With microprocessors getting faster every year, memory architectures must also improve to enhance the overall system performance. As rapid development in technology, speed and capacity are the major concern of the processors [1] [2]. For fast memory access architecture data has to be transferred faster than processor speed and transferring should be synchronized with the processor. This synchronization can be achieved by controller with time based control signals. So the DDR SDRAM controller can transmit data at both clock transition edges and that is synchronized with clock itself. Main important thing regarding to DDR SDRAM is available in low cost. So it is widely used in personal computers. So controller should be implemented based on synchronization. DDR SDRAM devices are low-cost, high-density storage resources that are widely available from many memory vendors.

From reference papers we observed that how to implement controller based on synchronization. Basic controller and different control signals with control operation is explained by finite state machine diagram [4].

Block Diagram of DDR SDRAM

The DDR SDRAM controller consists of Data path, Controller function unit, Address latch and Memory unit

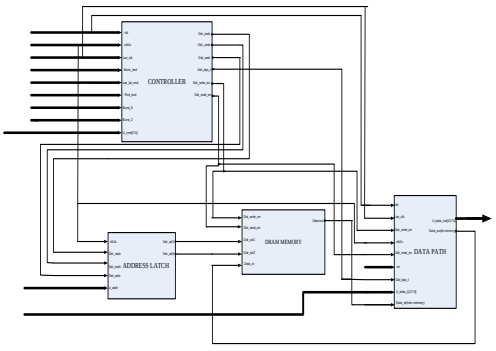

Fig. 1: schematic overview of DDR SDRAM controller architecture

Functional Blocks of DDR SDRAM:

Data Path Module:

Data path module is designed to provide double data transfer to memory per clock for a given single data per clock cycle based on the write enable and read

enable control signals which are from DDR SDRAM controller. This module is to improve data rate, which in turn to improve band width of the memory [4]. Main function of Data path module is sampling the user data and stores it, means sampling is nothing but converting double data rate to single data rate and single data rate to double data rate.

For Read access, data is sampled and then synchronized with the internal clock. And then data is transferred to the user interface at a rate of one-word per clock cycle. For Write access, data is received from the user interface at the rate of one word per clock and the data path then resynchronized the data and transfers them at double the normal rate.

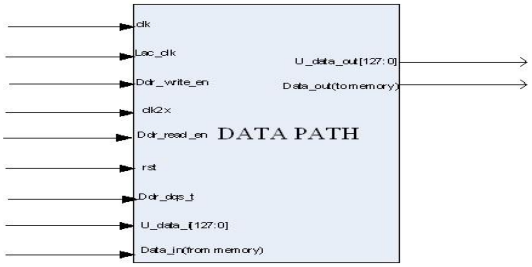

Fig. 2: Data path module pin diagram

Controller module:

DDR SDRAM should access external devices with high throughput and low latency. For that controller should have capability of generating high performance control signals to all other modules to perform control functionalities [5] . Controller consists of high performance timing and control state machine. Controller generates control signals based on user command given by user interface. These control signals mainly write enable, read enable and these signals will be given to data path module, address latch modules. The Data path module generates row address and column address based on these signals

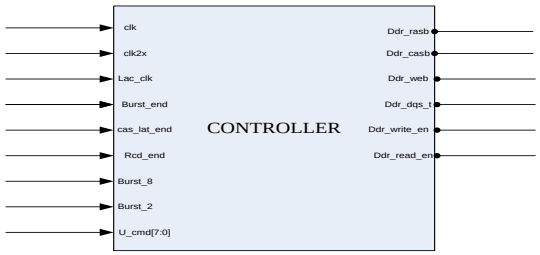

Fig. 3: Controller pin Diagram

Controller state machine diagram

State machine gives simplified and brief information regarding the controller. State machine explains about the states and on which input controller should change the state [6]. DDR SDRAM controller consists of 11 states and based on input command given from user state will be changed. To perform read operation controller should change initially from idle state to act state then to read state then read data. And finally reaches idle state again. For write operation, the data controller should change from idle state to write state and to write data state again it has to reach idle state finally [7][8]. In every state controller generated control signals are assigned to other modules to perform particular job assigned to them.

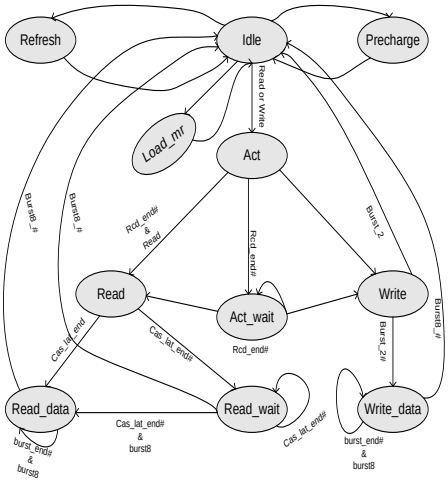

Fig. 4: Controller state machine diagram

Address latch:

Address latch module generates row (ddr_ad1), column (ddr_ad2) addresses based on control signals coming from the controller.

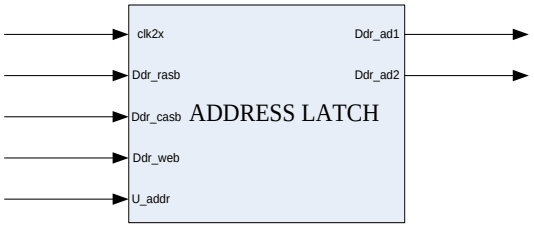

Fig. 5: Address latch module pin diagram

Address Latch FSM:

Initially address latch in idle state when reset applied. Based on control signals row address is transmitted and then column address is transmitted. Here once row address is transmitted then any number of times column address can be transmitted until ras_b signal is not changed.

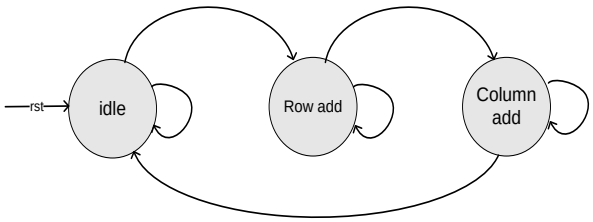

Fig. 6: State machine for Address latch

Memory module:

Data path module samples user data. This sampling of dada occurs at double the frequency of processor so memory should store this data. Memory module having inputs from both data path and address latch means address latch gives row, column address and data path module gives data word. Based on address memory module resolves the location and sampled the data and stores in it [9].

Here Data out pin is connected to data path and data in is coming from data path only [10]. Memory data is always transferred to data path only and data is received from again data path module.

Resource:

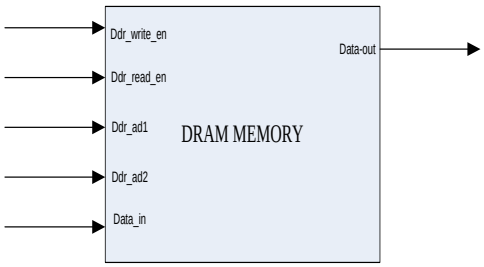

Fig. 7: DDR SDRAM memory module diagram

Simulation Results:

The Fig.8 represents simulation wave forms of data path module consists of 2, 4, 6 as user input data and 0,2,0,4,0,6 are ddr_dq data, which shows data generated twice per cycle then data is transferred into memory initially and then this data is fetched from memory by reading and again and transferred to user interface.

The controller works based on user interface command. For user command read controller changes the state from idle (0000), act(0100), act_wait(0101), read(0110), read_data(1001) again to idle(0000). For write operation Idle to again Idle through write and write_data states which is shown in the controller FSM diagram. Controller itself generates control signals along with rasb and casb and other signals are the outputs of controller at different states as shown in Fig. 9.

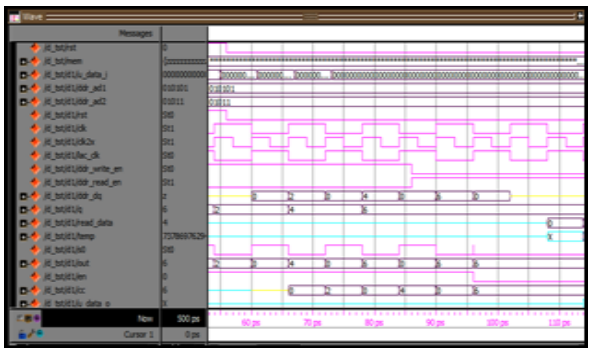

Fig. 8: Simulation waveforms for data read and write by data path module.

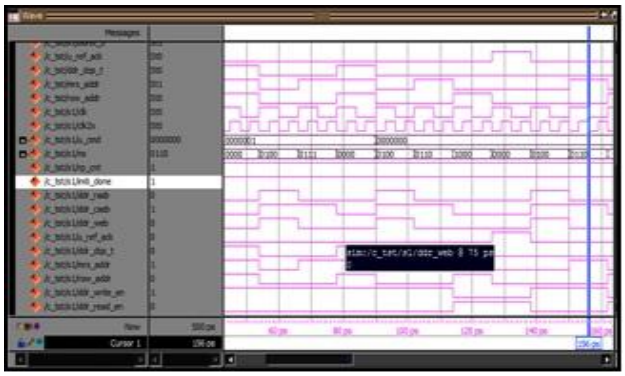

Fig. 9: Simulation waveforms for controller

The signals ddr_ad1, ddr_ad2 are the address signals generated based on the control signals like rasb and casb as shown in Fig.10. ddr_ad1 is generated at falling edge of rasb signal and ddr_ad2 is generated at falling edge of casb signal to make enable the row and column address in memory.

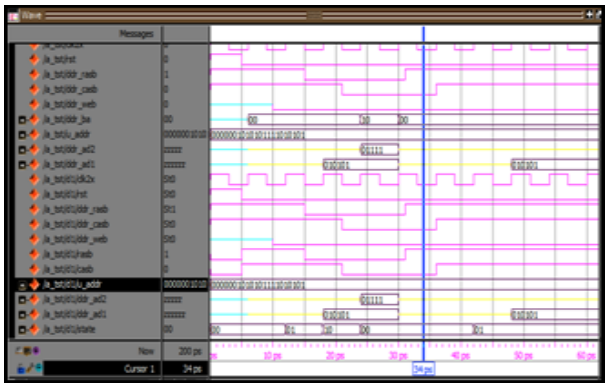

Fig. 10: Simulation waveforms for address generation by address latch

Based on Controller control signals, the address latch generates address enable signals, which are used to transfer double the data for a single clock. Here ddr_dq consists of data 1, 2, 3, 4, 5 and 6 each of 128 bits and the output data of data path module and the data 0,1,0,2,0,3,0,4,0,5,0,6,0 is transferred to memory. Here 0 data is transferring means 64 bit (higher bits) of data of value zero.

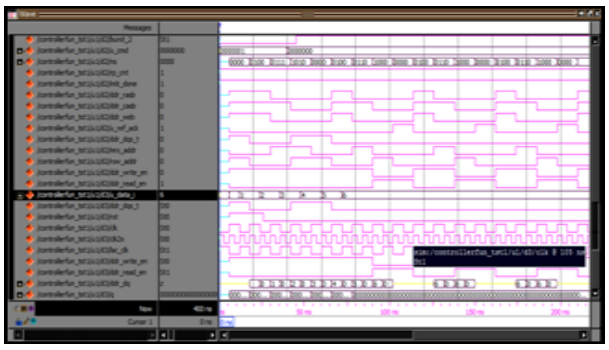

Fig. 11: simulation waveforms for controller read and write Operations

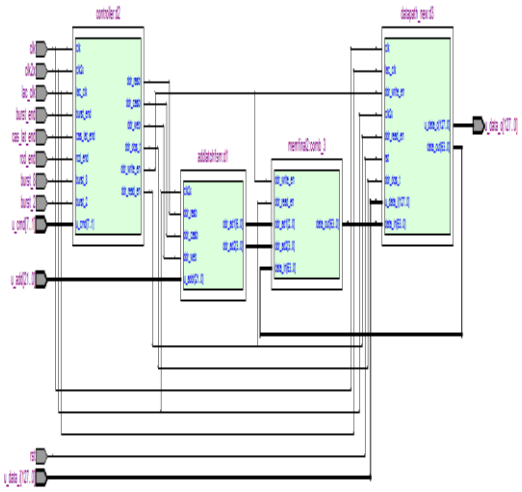

Fig. 12: RTL view of controller architecture

Conclusion:

In this paper an efficient DDR SDRAM controller is designed. Memory is designed in such a way that it operates at double the frequency of the processor's speed. The processor run at clock frequency then data transfer will be twice per each clock. In this controller data path is created to generate data at double the frequency means twice per each clock. In this way we can reduce the data bus size. And for every transition of system clock the data is transferring, also this controller consists of large number of buffers so still we have some amount delay.

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