

Low power optimization of full adder, 4-bit BCD adder.

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ABSTRACT

Micro-electronic devices are playing a very prominent role in electronic equipments which are used in daily life. For electronic equipment battery life is important. So, in order to reduce the power consumption we implement a Sleepy technique to the electronic circuits. Sleepy technique is also called as power gating technique. In the power gating structure, a circuit operates in two different modes. In the sleep mode, the sleep transistors are turned OFF to reduce the leakage power. In the active mode, the sleep transistors are turned ON and can be treated as the functional redundant resistances, as circuit is in operation mode the power leakage should not be more than the basic full adder. When a sleepy transistor is placed at V_{DD} , it is called as the "Header switch" and while it is placed near the ground, it is called as "Footer switch". Now in our project we implement this technique to the Full-adder and then it is used in 4-Bit Adder and 4-bit BCD Adder using 90nm scale technology. Without losing the CMOS logic a new full adder is designed by reducing the number of transistors which also leads to the reduction of chip size. In almost all electronic equipment full adder is used. So this project has been done with the aim of reducing the power consumption in the full adder circuit and implementing it in 4-Bit Adder and 4-Bit BCD Adder.

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Introduction:

Electronic devices such as mobile phones, cameras are used commonly these days. Its battery life span is of great concern. When mobile phone is operated in standby mode, certain programs of mobile phone or camera are turned off during active or talk mode but this doesn't stop the battery from getting depleted. This is because circuits which are de-activated by turning off certain programs still have leakage currents flowing through them. Even though the magnitude of leakage current is lesser than the normal operating current but leakage current erodes battery life over relatively long standby time whereas the normal operating current erodes battery life over relatively short talk time. Thus this is why low power circuits for mobile applications are of great interest. Implementation of adder cells to reduce the power consumption and to increase the speed has proved to be a worthy solution towards power reduction. Moreover, realization of adders with different approaches using CMOS technology widens the area of power reduction, performance of the adder cells can be evaluated by measuring the factors such as leakage power, active power in context to voltage and transistor scaling. Reducing the transistor's gate length when no voltage is applied at gate results in more leakage current between source and drain of the transistor which eventually results in the more power consumption.

Proposed Full Adder Circuits:

To minimize the number of transistors required to implement a given logic function can be done by pseudo NMOS and Pass-transistor but they result in more static power dissipation whereas on the other hand, dynamic logic style needs small silicon area for the implementation of complex function but charge leakage and charge refreshing reduces the operating frequency. In general, none of the mentioned styles can beat the CMOS style. The conventional CMOS adder has been shown in Figure: 1, it is the basic adder and all simulation results comparison has been done with it.

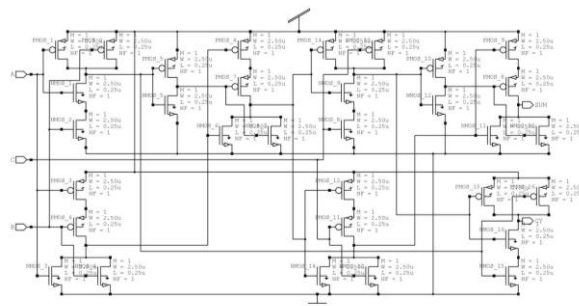


Figure: 1. Full adder

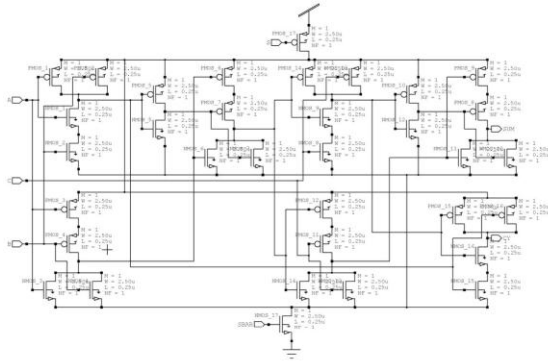


Figure: 1. Sleepy Full Adder

It consists of 32 transistors after incorporating PMOS pull up and NMOS pull down networks to produce desired outputs it got comprised of 34 transistors in Sleepy mode and 38 transistors in Sleepy Keeper mode. Here the sizing of transistors plays a vital role. Here, the transistor ratio of PMOS to NMOS has been kept 2:1. It is simulated in 90nm process; the results are provided in the Table: 1... Thus the adder circuit was modified with proper sizing using power gating technique and has been shown in Fig.2 power gating technique has been shown to reduce the leakage power by placing a sleep transistor between actual ground rail and circuit ground (virtual ground). Here low leakage NMOS is used as a sleep transistor. The width for NMOS is kept as 0.27um whereas for PMOS it's 0.54um and length is fixed for both i.e., 90nm as 90nm scale technology is used in this project. Sub threshold current is directly proportional to W/L ratio of transistor so the sizing reduces the standby leakage current to a very great extent. Adder design shown in Fig.2 is Sleepy Full Adder and Sleepy Keeper Full Adder in Fig.3 as the drawback in sleepy technique is avoided by using sleepy keeper technique without any change in power dissipation.

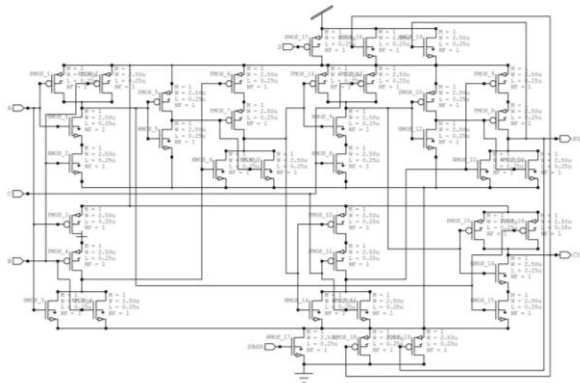


Figure: 2. Sleepy Keeper Full Adder

In active mode the dissipation of power of circuit is active power. This active power consists of dynamic power as well as the static power so it is being named as an active power. It is measured by making both the header and footer switches ON and then giving input vectors to the circuit and then the average power dissipation is calculated, then the results are compared as shown in Table-1. In static mode, since both the header and footer switches will be OFF, there will no V_{dd} supply and ground connected to the circuit, so the power dissipation will be very less, i.e., sub threshold leakage current will be present.

The major drawback in Sleepy technique is that it can't retain the values when it enters into sleep mode that is static mode, since there will be no supply the output values can't be

retained. For combinational circuits it may be fine but for sequential techniques it will fail as they depend on previous outputs and sleepy technique can't do it, so in order to avoid this discrepancy we go for Sleepy Keeper. In Sleepy Keeper technique in addition to sleep transistors another two transistors will be connected to retain the value in sleep mode as shown in the Figure-3. And the power dissipation will have no effect when compared to sleepy technique as shown in Table-1, so this technique is preferred over sleepy technique.

Proposed 4-bit Adder:

By using the full adders designed above, 4-Bit Adder is designed. The design shown in Figure-4, is designed by using basic full adder (Figure-1). The design shown in Figure-5 is similar for both sleepy and sleepy keeper technique but the internal circuitry of full adder will vary shown in Figure-2 and Figure-3.

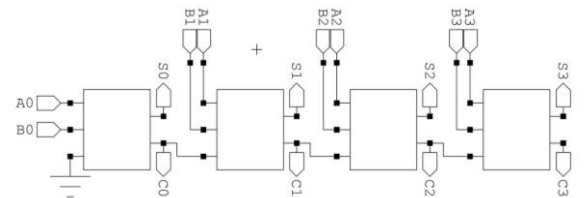


Figure: 3. 4-Bit Adder

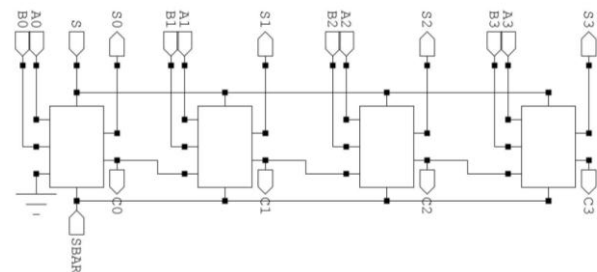


Figure: 4. Sleepy or Sleepy Keeper 4-Bit Adder

Proposed 4-Bit BCD Adder:

By using above 4 Bit adder circuit, 4-Bit BCD Adder is designed, the circuit shown in Figure-6 is the general 4-Bit BCD Adder and that circuit is again modified as shown in Figure-7, i.e., the AND-OR realization is modified with two 2-input NAND gates and one 3-input NAND gate. The design shown in Figure-8 is similar for both sleepy and sleepy keeper technique but the internal circuitry of full adder will vary shown in Figure-2 and Figure-3.

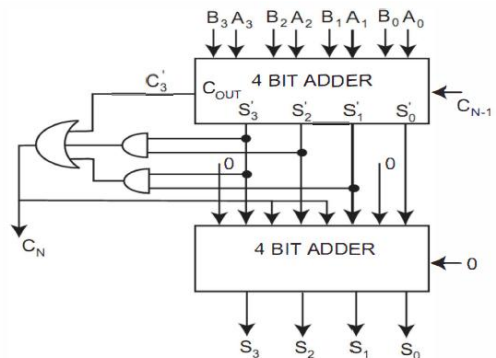
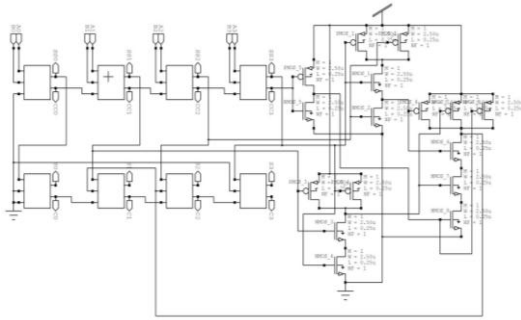
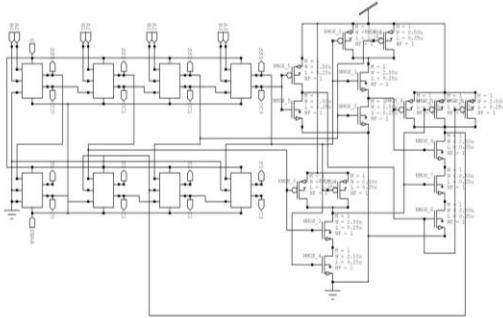


Figure: 5. 4-Bit BCD Adder

**Figure 6.** 4-Bit BCD Adder**Figure 7.** Sleepy or Sleepy Keeper 4-Bit BCD Adder

Simulation Results

The final power results of the 3 different full adder circuits for three different methods are shown in Table-1 and Table-2. The final power results of the 3 different circuits for three different methods are shown in Table-3. From that we can say that the average power of full adder and Sleepy full adder are very nearer to each other but when compared keenly, we can observe that Sleepy technique's power dissipation is less, so sleepy technique is better than basic CMOS full adder even in active mode. When we compare the results of Sleepy technique and Sleepy Keeper technique they remain same but the drawback of sleepy technique as explained earlier is rectified by using Sleepy keeper technique. This is how the justification to this project has been done.

Table: 1. Comparison of static power of full adders

Sl. No.	bits	basic full adder(nw)	sleepy full adder(nw)	sleepy keeper full adder(nw)
1	000	9.9237	0.25249	0.26451
2	001	11095	0.24805	0.25772
3	010	11.534	0.25059	0.26086
4	011	10.351	0.2308	0.23992
5	100	10.802	0.25057	0.26083
6	101	9.6189	0.23068	0.23979
7	110	8.852	0.22630	0.23439
8	111	10.023	0.22002	0.22203
Average Power		82.1996	1.9095	1.98005

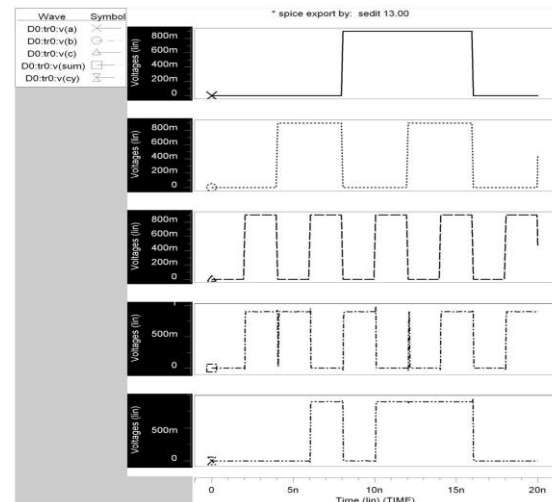
Table: 2. Comparison of active power of full adders.

Sl. No.	bits	basic full adder(nw)	sleepy full adder(nw)	sleepy keeper full adder(nw)
1	000	9.9237	9.9189	9.9189
2	001	11095	11.088	11.088
3	010	11.534	11.528	11.528
4	011	10.351	10.344	10.344
5	100	10.802	10.797	10.797
6	101	9.6189	9.6139	9.6139
7	110	8.852	8.8467	8.8467
8	111	10.023	10.016	10.016
Average Power		82.1996	82.1525	82.1525

Table: 3. Power analysis of different techniques

Circuit	Basic Cmos Technique	Sleepy Technique	Sleepy Keeper Technique
Full adder	82.1996	82.1525	82.1525
4-Bit Adder	39.929	39.910	39.910
4-Bit BCD Adder	82.059	82.024	82.024

Waveforms:

**Figure 9.** Basic Full Adder waveforms

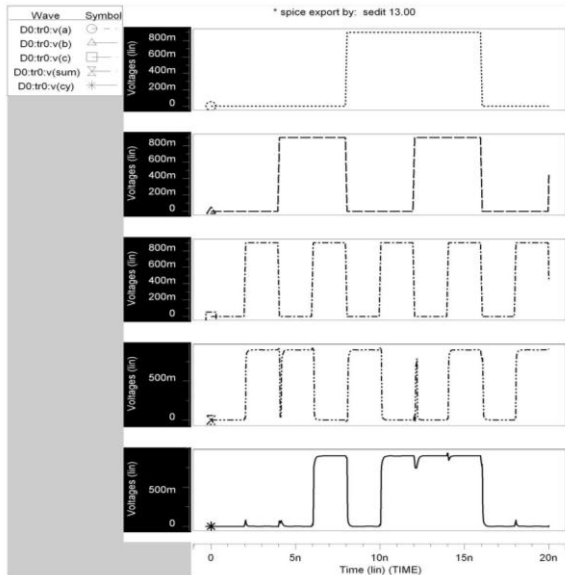


Figure 10.Active mode Sleepy Full adder

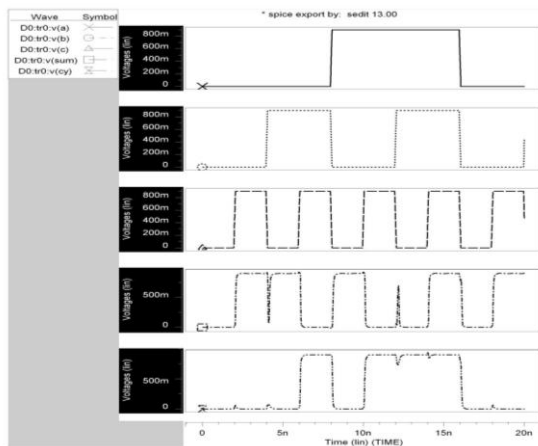


Figure 11.Active Sleepy Keeper Full Adder

Conclusion:

In this paper 1-bit full adder cell with Sleepy technique is implemented where a sleep transistor is added between actual ground rail and circuit ground. The device is turned off during sleep mode to cut-off the leakage path. For optimal performance, Sleepy Keeper technique has been implemented. The comparison of active power is done and it's observed that power is reduced as we move from conventional CMOS full adder cell to Sleepy and Sleepy Keeper technique. The implemented 1-bit full adders are designed using 90nm technology. So, from this we would like to propose the sleepy keeper technique for digital circuits for efficient performance of the device and for good battery life.

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